210067US2

"RESPONSE UNDER 37 CFR 1.116-
EXPEDITED PROCEDURE EXAMINING
GROUP 2819"

#14B
NE
Bell
12-17-02
Bell
3803

RECEIVED
NOV - 1 2002
TECHNOLOGY CENTER 2800

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

HIDEMASA ZAMA ET AL : EXAMINER: TAN, V.

SERIAL NO: 09/883,959 :

FILED: JUNE 20, 2001 : GROUP ART UNIT: 2819

FOR: SEMICONDUCTOR INTEGRATED :
CIRCUIT, LOGIC OPERATION
CIRCUIT, AND FLIP FLOP

AMENDMENT AFTER FINAL

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Official Action dated July 01, 2002, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claim 2 without prejudice or disclaimer.

Please amend claim 1 as follows:

1. (Twice Amended) A semiconductor integrated circuit comprising:

a plurality of gate circuits; and

a control circuit configured to control the operation of some gate circuits among said plurality of gate circuits,

each of said some gate circuits among said plurality of gate circuits including:

a logic circuit constituted by a plurality of first transistors; and